



## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **11007770 A**(43) Date of publication of application: **12.01.99**

(51) Int. Cl.

**G11C 11/409**  
**G11C 11/407**
(21) Application number: **09160707**(22) Date of filing: **18.06.97**(71) Applicant: **NEC IC MICROCOMPUT SYST LTD**(72) Inventor: **TASHIRO SHINYA**(54) **SEMICONDUCTOR MEMORY DEVICE**

COPYRIGHT: (C)1999,JPO

(57) Abstract:

**PROBLEM TO BE SOLVED:** To prevent data in a memory cell from being broken down so as to enhance its reliability in a semiconductor memory device which requires an I/O mask operation in a block write operation.

**SOLUTION:** In an I/O mask operation in a block write operation, a change in the precharging level of a common data line is suppressed so as to prevent data in a memory cell from being broken down, and, in addition, it is required to stabilize the level. In order to suppress a change in the precharging level of the common data line to a power-supply level -VTN or higher, a precharging part (a) is provided with MOST's 13, 14. Consequently, MOST's 8, 9 precharge respective P-data lines to a power-supply voltage level by means of a precharging control signal  $\phi_{\text{P}}$ . The NMOST's 13, 14 precharge the data lines to a voltage level in which threshold voltage portions of the NMOST's 13, 14 are subtracted from the power-supply voltage level, while the inverted signal of the precharging control signal  $\phi_{\text{P}}$  is used.

